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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,243	02/03/2004	Chad A. Cobbley	MICS:0078-4	2594
52142 7590 06/12/2008 FLETCHER YODER (MICRON TECHNOLOGY, INC.) P.O. BOX 692289 HOUSTON, TX 77269-2289				
EXAMINER				
PARKER, JOHN M				
ART UNIT		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/771,243

Applicant(s)

COBBLEY ET AL.

Examiner

John M. Parker

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 March 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-16 and 21-34 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 21-34 is/are rejected.
7) ☒ Claim(s) 11-16 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Miremadi et al. (US Pat. #5854507).

Regarding claim 21, Miremadi teaches the method of forming a semiconductor package comprising the acts of:

Forming a die stack, wherein the diestack comprises an adhesive on at least one surface of a first die, wherein forming the die stack comprises mechanically coupling the die stack together via the adhesive [fig. 8, 38] and electrically coupling the die stack together via bond wires or conductive balls [fig. 4, 43 solder balls are described in column 6, lines 28-50].

Placing the die stack on a substrate [fig. 9, 70].

Miremadi fails to teach moving said die stack to a temporary position prior to moving it to substrate. However, it would have been obvious to one of ordinary skill in the art to place the completed die stack upon a temporary holding surface because the placing of the die stack on the temporary surface merely adds complexity to the process of Miremadi. The process of Miremadi would have been expected by one of ordinary skill in the art to be performed equally well by taking different paths for the stack

because the stack is ultimately placed in the desired position in all such processes and the intermediate placing on a temporary surface would not be expected to materially alter the final positioning.

Regarding claim 22, Miremadi discloses the method as set forth in claim 21, comprising the act of curing the die stack before the act of picking the die stack [column 7, lines 36-67, fig. 8 shows the stack prior to being placed on a substrate, therefore it was cured prior to being picked from the temporary surface].

Regarding claim 23, Miremadi fails to teach the act of testing the die stack. however, the background of Miremadi teaches it is well known to test a chip prior to being mounted on a PCB (substrate) [column 1, lines 23-25].

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Miremadi's background into the method of Miremadi by testing the die stack prior to mounting on the substrate. The ordinary artisan would have been motivated to modify Miremadi in the manner set forth above for at least the purpose of ensuring a functional die stack and saving manufacturing costs related to mounting faulty die.

Regarding claim 24, Miremadi fails to teach the specific use of a tape reel as the temporary holding surface for the die stack. however, the use of tape reels are common in die transfer processes. the examiner takes official notice that tape reels were known to be used as temporary holding surfaces of die stacks at the time of applicants invention.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Miremadi and what is well known in the art to enable the method step of using a tape reel as the temporary holding surface to be performed according to the known method because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative, suitable or useful methods of performing the disclosed processing step of holding a die stack. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Regarding claim 25, Miremadi fails to teach the specific use of a gel pack as the temporary holding surface for the die stack. however, the use of gel packs are common in die transfer processes. the examiner takes official notice that gel packs were known to be used as temporary holding surfaces of die stacks at the time of applicants invention.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Miremadi and what is well known in the art to enable the method step of using a gel pack as the temporary holding surface to be performed according to the known method because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative, suitable or useful methods of performing the disclosed processing step of holding a die stack. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Regarding claim 26, Miremadi fails to teach the specific use of a tray as the temporary holding surface for the die stack. however, the use of trays are common in

die transfer processes. the examiner takes official notice that trays were known to be used as temporary holding surfaces of die stacks at the time of applicants invention.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Miremadi and what is well known in the art to enable the method step of using a tray as the temporary holding surface to be performed according to the known method because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative, suitable or useful methods of performing the disclosed processing step of holding a die stack. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Regarding claim 27, Miremadi fails to teach the specific use of a wafer as the temporary holding surface for the die stack. however, the use of wafers are common in die transfer processes. the examiner takes official notice that wafers were known to be used as temporary holding surfaces of die stacks at the time of applicants invention.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Miremadi and what is well known in the art to enable the method step of using a wafer as the temporary holding surface to be performed according to the known method because one of ordinary skill in the art would have been motivated to look to analogous art teaching alternative, suitable or useful methods of performing the disclosed processing step of holding a die stack. Art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Regarding claim 28, Miremadi discloses the method as set forth in claim 21, wherein the die stack comprises at least two semiconductor die [fig. 8]

Regarding claim 29, Miremadi teaches the method as set forth in claim 21 wherein the die stack comprises at least three semiconductor die [fig. 9].

Regarding claim 31, Miremadi discloses the method as set forth in claim 21, comprising the acts of:

Applying the adhesive between each die in the die stack, the adhesive being curable at a first temperature [fig. 8, 38 the first adhesive is used as a thermal conductor, therefore it must have a very high temperature] ; and

Applying the second adhesive between the die stack and the substrate, the second adhesive being curable at a temperature lower than the first temperature [fig. 9, 67 (19 in fig. 8) column 8, lines 20-35, the solder is reflowed while the layer 38 still acts as a heat transport layer].

Regarding claim 32, Miremadi teaches the method as set forth in claim 21 comprising the act of using the die stack on the substrate to form an integrated circuit package [all the stacks created are IC packages, columns 3 and 4, lines 60-67 and 1-21 respectively].

Regarding claim 33, Miremadi discloses the method as set forth in claim 32, comprising the act of electrically coupling the integrated circuit package to a processor to form an electronic system [column 4, lines 7-10].

Regarding claim 34, Miremadi teaches the method as set forth in claim 21, wherein at least one die in the die stack comprises a memory die [column 4, lines 1-10].

Claim 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Miremadi et al. (US Pat. #5854507) in view of Huang et al. (US Pat. #6753205).

Regarding claim 30 Miremadi fails to teach a die stack formed in a shingled configuration. However, Huang teaches an integrated circuit package with a singled configuration [fig. 2 and 5].

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Huang into the method of Miremadi by stacking the chips in a shingled configuration. The ordinary artisan would have been motivated to modify Miremadi in the manner set forth above for at least the purpose of being able to package integrated circuit chips of various relative sizes [Huang, column 2, lines 45-47].

Allowable Subject Matter

Claims 11-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 11-16 and 21-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Parker whose telephone number is (571)272-8794. The examiner can normally be reached on Monday - Friday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/George Fourson/
Primary Examiner, Art Unit 2823

/J. M. P./
Examiner, Art Unit 2823